Peter Fabinski

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Objective

To apply knowledge of Computer Engineering and gain experience and skills in a constructive environment.

Education

- **Rochester Institute of Technology** **Rochester, NY**
  BS/MS Dual Degree in Computer Engineering 2017 - 2022
  GPA: 4.00/4.00
  Awards: Dean's List all semesters, RIT Presidential Scholarship
  Courses: Design & Test of Multi-core Chips
  Reconfigurable Computing
  Digital IC Design
  Complex Digital Systems Verification
  Real-time & Embedded Systems
  Computer Architecture

Skills

- **Programming Languages:** C, VHDL, SystemVerilog, UVM, Python, Perl, ARM & MIPS ASM, Java, Bash
- **Software:** Vivado, SimVision, MGC Pyxis, Calibre, Quartus, ModelSim, Altium, Git, PSpice, ROS, Office
- **Hardware:** FPGA, Microcontroller, Oscilloscope, Multimeter, Signal Generator, Soldering Iron, PC hardware
- **Other:** Extensive PC assembly and maintenance experience; practical knowledge of networking; experience managing mail and web servers on Linux

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Experience

- **Critical Link, LLC** **Syracuse, NY**
  Intern Engineer May - December 2019
  - Managed the review and release processes for various products, PCA/PCB designs, and documents.
  - Reviewed additions/changes to company component model library (footprints, symbols, and parameters), verifying against information from datasheets.
  - Rewrote Python script for bulk component information gathering to use an API instead of web scraping.
  - Documented steps to modify existing PCAs to match new revisions, as well as creating documentation for unreleased test fixtures.
- **Microworx Computer Sales and Service** **Rochester, NY**
  Jr. System Builder 2016 - 2019 (15 months total)
  - Assembled, configured, and tested numerous desktop computers for enterprise and personal environments. Followed an established build procedure to record parts used, track progress, and ensure that completed PCs function correctly.
  - Began development of a Visual Basic + SQL inventory tracking system to replace paper sign-out sheets for high-value components.
  - Worked on fixes and improvements to the internal Perl CGI-based ticketing system, as well as the quote-creation tool for new PCs.

Projects/Labs

- Produced coverage-driven randomized SystemVerilog and UVM testbenches for DTMF receiver module.
- Designed and tested MAC unit w/BIST (HDL synthesis, autolayout) and 4-bit full adder (manual layout).
- Created FPGA-based image-filtering system with both VHDL and high-level synthesis implementations.
- Used VHDL to create pipelined MIPS processor, determining maximum clock frequency by timing simulation.
- Followed Agile process in 4-person team to develop a fully-featured Checkers webapp in Java.
- Installed and continue to maintain a Linux-based mail/web server with SSL, as well as other applications.